METHODS, APPARATUS AND SOFTWARE FOR IMPROVING SMI LATENCY ON SYSTEMS USING TIMING-SENSITIVE REGISTERS

ABSTRACT

A system, method and software that provides for improved system management interrupt (SMI) latency the present invention includes a real-time clock, and a register file containing one or more timing sensitive registers. An index and data register is provided for accessing the timing sensitive registers in the register file. An update-in-progress status bit determines a certain fixed period of time for which the timing-sensitive registers are valid. A retriggerable, fixed duration timer is triggered by reads of zero from the update-in-progress status bit. A latch is provided that is set if the timer is running when a system management interrupt is asserted and cleared when SMI is deasserted. A mechanism is provided for reading the output status of the latch. A timer is provided that is triggered by reading zero from a first register location. A status latch is provided for storing the status of the timer, which status is read using a status bit. SMI handling code is provided that reads the status latch, and if the status latch is zero, exits the SMI handling code, and if the status latch is non-zero, writes 0A to I/O location 0x70 of a second register location, reads I/O location 0x71 from a third register location, and if bit 7 of the value read from the third register location is set, repeats the previous two steps until the value of bit 7 is not set, and then exits the SMI handling code.